Amendments to the Claims

The following listing of the claims will replace all prior versions, and listings of the claims in the application:

Listing of Claims

1-21 (Canceled)

22. (Currently amended) A method for implementing a class of NxN expanders each serving a connection request to route m incoming signals, $m \leq N$, and for enabling the service of any connection request in a nonblocking way on the condition that the connection request is compliant to certain constraints, the method for each of the expanders comprising:

configuring a switch defined by a set of connection states and having an array of N input ports with N distinct input addresses and an array of N output ports with N distinct output addresses wherein the m incoming signals arrive at m input ports determining m active input addresses and are destined for a total of n, $m \leq n \leq N$, distinct output ports determining n active output addresses, and wherein said constraints on the connection request are that: (1) the m active input addresses are consecutive upon a rotation of the ordering of the N input addresses, and (2) for any two active input addresses i and j and any two active output addresses p and q such that i is being connected to p and j is being connected to q, if i precedes j with respect to the rotated ordering, then $p < q$, and

routing the incoming signals from said m input ports to said n distinct output ports by activating one of the connection states such that the activated one of the connection states accommodates the connection request subject to said constraints on the connection request,

said class excluding (i) those having a switch constructed from the banyan network of expander cells prepended with the shuffle exchange and (ii) those having a switch constructed from the shuffle-exchange network of expander cells prepended with the shuffle exchange.

23. (Previously presented) The method as recited in claim 22 wherein the configuring includes constructing the switch as an NxN k-stage switching network composed of k stages of

nodes, an interstage exchange between any succeeding two of the k stages, an input exchange and an output exchange, and wherein each node is filled with another switch.

24. (Previously presented) The method as recited in claim 22 wherein the configuring includes constructing the switch as an NxN k-stage switching network composed of k stages of nodes, an interstage exchange between any succeeding two of the k stages, an input exchange and an output exchange, and wherein each node is filled with an expander.

25. (Previously presented) The method as recited in claim 22 wherein the configuring includes constructing the switch as a two-stage interconnection network composed of a first stage of nodes being the input nodes and a second stage of nodes being the output nodes, an interstage exchange, and an input exchange corresponding to the interstage exchange prepended to the network, and wherein each node is filled with an expander.

26. (Previously presented) The method as recited in claim 22 wherein the configuring includes constructing the switch as an x2 interconnection network having nodes and wherein each node is filled with an expander.

27. (Previously presented) The method as recited in claim 22 wherein the configuring includes constructing the switch as an x2 interconnection network having nodes and wherein the nodes are filled with a plurality of expanders.

28. (Previously presented) The method as recited in claim 22 wherein the configuring includes constructing the switch as a recursive x2 interconnection network having nodes and wherein each node is filled with an expander.

29. (Previously presented) The method as recited in claim 22 wherein the configuring includes constructing the switch as a recursive x2 interconnection network having nodes and wherein the nodes are filled with a plurality of expanders.

30. (Previously presented) The method as recited in claim 22 wherein the configuring includes constructing the switch as a recursive x2 interconnection network having nodes and wherein each of the nodes is a cell and each cell is filled with a 2x2 expander.

31. (Previously presented) The method as recited in claim 30 wherein the 2x2 expander is an expander cell.

32. (Previously presented) The method as recited in claim 22 wherein the configuring includes constructing the switch as a recursive x2 interconnection network of cells with each cell filled with a 2x2 expander.

33. (Previously presented) The method as recited in claim 32 wherein the 2x2 expander is an expander cell.

34. (Previously presented) The method as recited in claim 22 wherein the configuring includes constructing the switch as a banyan-type network whose trace and guide are both monotonically increasing and wherein each of the 2x2 nodes of the banyan-type network is filled with a 2x2 expander.

35. (Currently amended) The method as recited in ~~claims from~~ claim 34 wherein the 2x2 expander is an expander cell.

36. (Previously presented) The method as recited in claim 22 wherein the configuring includes constructing the switch as a recursive plain 2-stage interconnection network of ceils prepended with a swap exchange and wherein each cell of the network is filled with a 2x2 expander.

37. (Previously presented) The method as recited in claim 36 wherein the 2x2 expander is an expander cell.

38. (Previously presented) The method as recited in claim 22 wherein the configuring includes constructing the switch as a divide-and-conquer network of cells prepended with a swap exchange and wherein each cell of the network is filled with a 2x2 expander.

39. (Currently amended) A class of NxN expanders each serving a connection request to route m incoming signals, $m \leq N$, and for enabling the service of any connection request in a nonblocking way on the condition that the connection request is compliant to certain constraints, each of the expanders comprising:

a switch defined by a set of connection states and having an array of N input ports with N distinct input addresses and an array of N output ports with N distinct output addresses wherein the m incoming signals arrive at m input ports determining m active input addresses and are destined for a total of n, $m \leq n \leq N$, distinct output ports determining n active output addresses, and wherein said constraints on the connection request are that: (1) the m active input addresses are consecutive upon a rotation of the ordering of the N input addresses and (2) for any two active input addresses i and j and any two active output addresses p and q such that i is being connected to p and j is being connected to q, if i precedes j with respect to the rotated ordering, then $p < q$, and

control circuitry, coupled to the switch, for routing the incoming signals from said m input ports to said n distinct output ports by activating one of the connection states such that the activated one of the connection states accommodates the connection request subject to said constraints on the connection request,

said class excluding (i) those having a switch constructed from the banyan network of expander cells prepended with the shuffle exchange and (ii) those having a switch constructed from the shuffle-exchange network of expander cells prepended with the shuffle exchange.

40. (Previously presented) The expander as recited in claim 39 wherein the switch is constructed by an NxN k-stage switching network composed of k stages of nodes, an interstage exchange between any succeeding two of the k stages, an input exchange and an output exchange, and wherein each node is filled with another switch.

41. (Previously presented) The expander as recited in claim 39 wherein the switch is constructed by an NxN k~stage switching network composed of k stages of nodes, an interstage exchange between any succeeding two of the k stages, an input exchange and an output exchange, and wherein each node is filled with another expander.

42. (Previously presented) The expander as recited in claim 39 wherein the switch is constructed from a two-stage interconnection network composed of a first stage of nodes being the input nodes and a second stage of nodes being the output nodes, an interstage exchange, and an input exchange corresponding to the interstage exchange prepended to the network, and wherein each node is filled with another expander.